FPGA Implementation of LDPC Encoder for Terrestrial Television

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Abstract— *The increasing data rates in digital television networks increase the demands on data capacity of the current transmission channels. Through new standards, the capacity of existing channels is increased with new methods of error correction coding and modulation. In this work, Low Density Parity Check (LDPC) codes are implemented for their error correcting capability. LDPC is a linear error correcting code. These linear error correcting codes are used for transmitting a message over a noisy transmission channel. LDPC codes are finding increasing use in applications requiring reliable and highly efficient information transfer over noisy channels. These codes are capable of performing near to Shannon limit performance and have low decoding complexity. LDPC uses parity check matrix for its encoding and decoding purpose. The main advantage of the parity check matrix is that it helps in detecting and correcting errors which is a very important advantage against noisy channels. This work presents the design and implementation of a LDPC encoder for transmission of digital terrestrial television according to the Chinese DTMB standard. The system is written in Verilog and is implemented on FPGA. The whole work is then verified with the help of Matlab modelling.*

Keywords— LDPC, BCH, FPGA, DTMB, Scrambler, LFSR.

I. INTRODUCTION

In digital data transmission or storage systems, messages transmitted or stored often go through a channel or storage medium that introduces noise that may corrupt the original message. Forward error correction (FEC) codes were introduced in order to solve this problem. In the case of a data transmission communication system, an encoder is introduced at the transmitter to encode the message bits by adding redundancy to the message. This redundancy is transmitted to the receiver along with the message. At the receiver, the received message is decoded in hopes of correcting the errors that may have been introduced during the transmission through the channel and retrieving the original message. According to Shannon's theorem [1], no matter how noisy the communication channel is, there exists an error correction code that can make the probability of error small for a transmission rate. In recent years, one of the most successful types of codes in doing so has been LDPC codes. LPDC codes were introduced in 1960 by Gallager. Due to its advantages, it was adopted by many standards to be used as a FEC for Digital Video Broadcasting. M.Sakurai [2] has proposed the implementation of ISDB standard which uses RS coding as a FEC. Jian-yun Zheng ,Jing Gao [3] have proposed the use of Turbo coding as the FEC for DVB standard. Among all the different forward error correcting codes LDPC codes are found and proved to be the one that achieves maximum Shannon limit. The Chinese make use of LDPC encoder in their DTMB standard. The encoder is implemented in FPGA. Field Programmable Gate Array is a Integrated Circuit(IC) consisting of configurable logic elements that be altered as per the requirement. Verilog is a type of HDL language which is used to implement the design in FPGA. As opposed to Application Specific Integrated Circuit (ASIC) FPGA can be reprogrammed after the manufacturing process as per the requirement. This work presents the FPGA Implementation of LDPC encoder.

II. BASIC WORKING

The messages which are to transmitted are in digital format, are given using the switch interface in FPGA. The messages are scrambled and are sent to the LDPC encoder. The encoding process is done with the help of parity check matrix which is generated using Matlab. The messages are then sent to the BCH encoder. Data packets which are the output of LDPC encoder when fed to BCH encoder gives the data in frames.

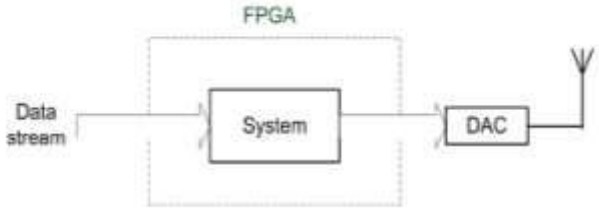


Fig.1: Basic Block Diagram

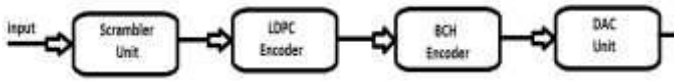


Fig.2: System Block Diagram

The final output is then given to DAC module to convert the given digital signal to analog for transmission. We can see the encoded output in the Xilinx software and in the LEDs present in the FPGA kit.

III. EXISTING METHODOLOGY

In India here we use DVB-T standard. This standard uses RS encoding as forward error correcting code. With this encoding algorithm Shannon limit cannot be reached, which is big disadvantage. It is difficult to implement this encoder in hardware. The complexity of implementing RS encoder is more when compared to LDPC encoder. The receiver complexity is also more. So when comparing both the codes LDPC is better due its performance and it consumes less resources.

IV. PROPOSED SYSTEM

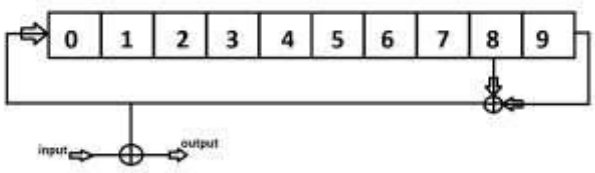
To design a LDPC encoder which forms the part of the Chinese DTMB standard. By achieving Shannon limit with the help of LDPC codes we will be able to send more information signals or we can get a better quality picture like a HD picture all within the same bandwidth.

V. METHODOLOGY

Methodology involves three main stages. The first stage involves acquiring the input message from the user via switch interfacing in the FPGA kit. The second stage involves scrambling the data with the help of Scrambler unit. The third stage involves encoding the scrambled data with the help of LPDC and BCH encoder. Lastly the encoded codeword from the encoder stage is converted to analog signal using DAC module for transmission.

A. Scrambler Unit*:*

Scrambler is a device used in telecommunication that helps in randomizing data.



Scrambler unit is basically a set of LFSR s connected together, with each having an initial seed value and a logical operation is present between the registers. In this case we are using a XOR logic gate and the output is fed back as input to the first linear feedback shift register. Scrambling is necessary because the transmitter design does not have any constraints with the inputs. If a string of zeroes is obtained it may cause some doubts at the receiver side. So with scrambler such problems can be eliminated.

B. LDPC Encoder

The first step of LDPC encoding is the generation of Parity Check Matrix (H matrix). With 'n' defined as the total length of the codeword and 'k' defining the number of message bits. So n-k gives the number of parity bits. With these basic information we can create the parity check matrix using Matlab.

$H= [I_{n-k} \mid P^T]$, where I is identity matrix and order of the overall matrix is (n-k, n)

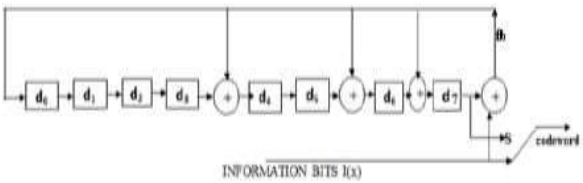
Generator matrix can be derived from H matrix using

$G= [P \mid I_k]$, where I is identity matrix and order of overall matrix is (k, n).

The codeword is derived using the generator matrix. The parity check matrix is very important since it is used for error correction and finally retrieve the message back from the codeword. Parity check matrix is used to find the syndrome for corresponding error pattern which helps in getting back the transmitted message without any error.

C. BCH Encoder

The first part of BCH encoder is parallel to serial converter. The encoded word from the previous encoder is sent as input to the BCH encoder. The data packets are converted into frames. The second part of the BCH encoder involves shift registers. After the parallel to series conversion the bits are fed as shown below



The last stage of BCH encoder involves serial to parallel converter. The encoded bits are converted to a parallel fashion and are displayed in the on board LED s.

D. DAC module

The final block in the whole system is digital to analog converter. The encoded bits are now converted into analog signal for transmission. The analog output can be seen in cathode ray oscilloscope (CRO).

VI. RESULTS

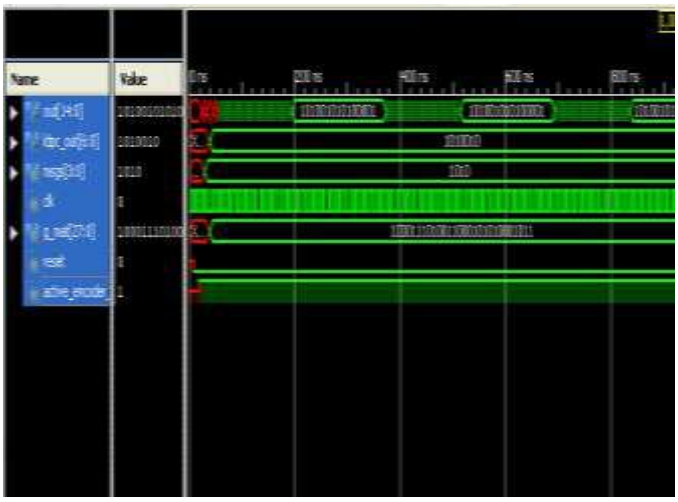


Fig.3: Codeword Generated in Isim Simulator

Fig.3 Shows the complete output stage by stage when an input message is entered via the switching interface in the FPGA board.

Fig.4: RTL Schematic

Fig.4 shows the RTL schematic of the total logic of the encoder through logic circuit elements.

Fig.5: Technology Schematic

Fig.5 shows the technology schematic i.e. the total logic of the encoder inside the Xilinx FPGA chip.

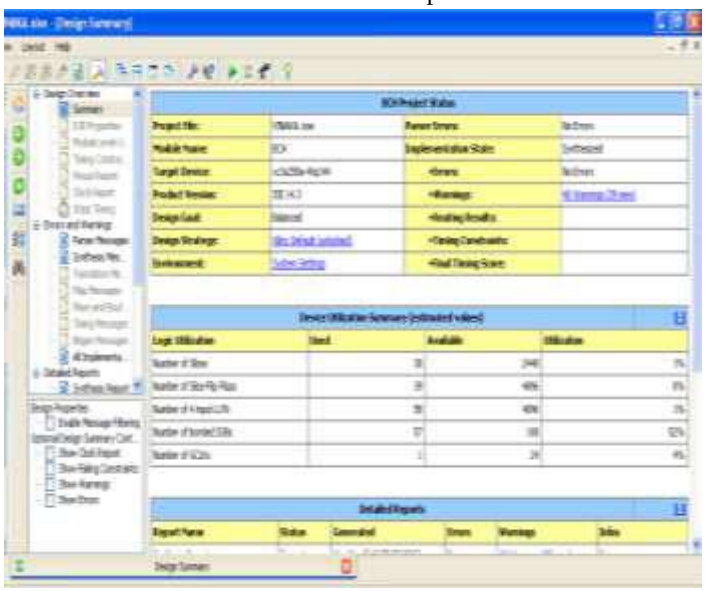


Fig.6: Design Summary

Fig.6 shows the hardware utilization of the logic. It shows the number of slices,flip-flops used.

VII. CONCLUSION AND FUTURE WORK

Thus by implementing LDPC coding in our television standards we can achieve more transmission rate or reach Shannon limit i.e. zero error probability. So we will be able to send more signals or we can get a better quality picture in the same allocated bandwidth. This is a huge improvement over other codes. The complexity involved is also less when compared to other codes. So LDPC encoding is a technique with high advantages that can be integrated to the standard we use. The work can be extended by improving the length of the codes to higher orders and can we can also add a decoding platform to get back our message.

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